REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested in light of the present Supplemental Amendment and the Amendment of December 24, 2003 that was entered as directed by the RCE filed February 25, 2004.

Claims 25-34 are pending for examination in this application. Claims 33 and 34 are being added to better clarify the full scope of the present invention without the introduction of any new matter. Note, for example, FIGS. 44 and 45 and the corresponding description of the specification at page 69, line 14 to page 71, line 13 as to Claim 33 and note, for example, the description in the specification at page 69, lines 17 and 18 permitting one or all (at least one IEGT chip includes one, two, etc.) to have a current sense function as to Claim 34.

The outstanding rejection of Claims 25-32 under 35 U.S.C. § 103(a) as being unpatentable over <u>Yanagisawa et al</u> (U.S. Patent No. 5,874,750, <u>Yanagisawa</u>) in view of <u>Takeda et al</u> (1998 International Symposium article, <u>Takeda</u>) is clearly not applicable to new Claims 33 and 34 any more than it is reasonably applicable to Claims 25-32 for the reasons set forth in the December 24 Amendment.

In this respect, <u>Yanagisawa</u> at best teaching an IGBT having an emitter electrode plate 16 and a collector electrode plate to form a pressure-contact type IGBT which comprises a <u>single-emitter structure</u> and an emitter sensing terminal ES directly connected with the single emitter <u>for monitoring the emitter voltage</u> (which is a potential difference between the emitter on the IGBT chip and the ground of the gate circuit), so that the emitter sensing terminal is not influenced by inductance between the signal emitter and the emitter sensing terminal. In operation, <u>a voltage</u> (a potential difference) of the emitter on the IGBT chip and the ground of the gate is taken out at the emitter sensing terminal and <u>no substantial current flows through the emitter sensing terminal</u>. Clearly, there is no extraction to any external protection circuit

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of any part of an emitter current flowing through a current emitter of any IEGT chip as both

new claims 33 and 34 further require.

As further noted in the December 24 Amendment, <u>Takeda</u> shows no more than a

trench gate type IEGT having a multi-emitter structure for an over current limiting circuit.

Therefore, it is again clear that Yanagisawa shows no more than a pressure-contact

type IEGT having an emitter voltage sensing terminal connected to a single emitter and that

Takeda shows no more than an IEGT having a double-emitter structure and does not show a

pressure-contact type IEGT having a current sense emitter. Accordingly, even if the structure

taught by Yanagisawa were to be modified by or combined with that shown by Takeda, the

pressure-contact type IEGT having a current sense emitter recited in the amended

independent claims is not the result and no prima facie case of obviousness has been

established as to the subject mater of new Claims 33 and 34, much less previously presented

Claims 25-32.

In view of the above comments and the further comments set forth in the December

24 Amendment, it is respectfully submitted that no issues remain outstanding relative to the

present application, which is, therefore, clearly in condition for formal allowance.

Accordingly, an action to that effect is respectfully requested.

Respectfully submitted,

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